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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/727,744	12/01/2000	Lawrence Richard Fontaine	RA 5312 (1028.1132101)	4178

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/727,744	FONTAINE ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 12-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-27* is/are allowed.

6)☒ Claim(s) *1,3-10 and 12-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-10, and 12-27 have been considered. Claims 1 and 10 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: After-Final Amendment as received on 24 March 2005 and RCE as received on 05 May 2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 5-10, 12-13, and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Col et al., U.S. Patent Number 6,338,136 (herein referred to as Col) in view of Cocke et al., U.S. Patent Number 3,577,189 (herein referred to as Cocke).

5. Referring to claim 1, Col has taught a method for processing a conditional jump instruction in a pipelined instruction processor, the method comprising:

a. Generating at least one status bit based on a digital value to be stored, the at least one status bit relating to a particular condition of a conditional jump instruction and specifying if the particular condition of the conditional jump instruction is satisfied or not (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4,

lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B);

b. Storing the digital value and the at least one status bit to a memory (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

c. In response to a conditional jump instruction, reading from the memory the digital value and the at least one status bit to resolve whether the condition of the conditional jump instructions is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

6. Col has not taught to resolve whether the condition of the conditional jump instruction is satisfied before the conditional jump instruction reaches an arithmetic logic stage of the pipelines instruction processor. Cocke has taught to resolve whether the condition of the conditional jump instruction is satisfied before the conditional jump instruction reaches an arithmetic logic stage

of the pipelines instruction processor (Cocke Abstract; column 1, lines 41-57; column 1, line 74 to column 2, line 20; column 2, lines 29-37 and 59-75; column 3, lines 37-47; column 4, lines 10-17; Figure 5; Figure 6; and Figure 7). In regards to Cocke, the "BR if a and b" is the condition of a conditional branch that is resolved before the actual branch portion of the instruction is executed with the exit instruction. In other words, the condition of a conditional branch instruction is resolved prior to the arithmetic logic stage when the actual branching or jumping portion of a conditional branch or jump is executed, e.g. the condition is resolved prior to the arithmetic logic stage calculating the target of the branch instruction. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Cocke, that Cocke's method of branching improves performance (Cocke column 1, lines 41-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the branching method of Cocke to improve processor performance.

7. Referring to claim 3, Col has taught wherein the at least one status bit is read from memory at the same time as the digital value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

8. Referring to claim 5, Col has taught wherein the at least one status bit is set high if the digital value is zero (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14,

lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

9. Referring to claim 6, Col has taught wherein the at least one status bit is set high if the digital value is a positive value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

10. Referring to claim 7, Col has taught wherein the at least one status bit is set high if the digital value is negative (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

11. Referring to claim 8, Col has taught wherein the at least one status bit is set high if the digital value is a non zero value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27;

column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

12. Referring to claim 9, Col has taught wherein the at least one status bit is set high based on the value of the least significant bit of the digital value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

13. Referring to claim 10, Col has taught in a pipelined instruction processor that executes instructions including conditional jump instructions, one or more of the conditional jump instructions reading a digital value from memory to determine if the condition of the conditional jump instruction is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B), the improvement comprising:

a. Status bit generator for generating at least one status bit based on a digital value, the at least one status bit indicating if a predetermined condition of a conditional jump instruction is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines

18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B);

b. Storing means for storing the digital value and the at least one status bit to the memory (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

c. Conditional jump processing means, activated in response to the execution of a conditional jump instruction, the conditional jump processing means reading from the memory the digital value and the at least one status bit to resolve whether the condition of the conditional jump instruction is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

14. Col has not taught to resolve whether the condition of the conditional jump instruction is satisfied before the conditional jump instruction reaches an arithmetic logic stage of the pipelines instruction processor. Cocke has taught to resolve whether the condition of the conditional jump instruction is satisfied before the conditional jump instruction reaches an arithmetic logic stage of the pipelines instruction processor (Cocke Abstract; column 1, lines 41-57; column 1, line 74 to column 2, line 20; column 2, lines 29-37 and 59-75; column 3, lines 37-47; column 4, lines 10-17; Figure 5; Figure 6; and Figure 7). In regards to Cocke, the "BR if a and b" is the condition of a conditional branch that is resolved before the actual branch portion of the instruction is executed with the exit instruction. In other words, the condition of a conditional branch instruction is resolved prior to the arithmetic logic stage when the actual branching or jumping portion of a conditional branch or jump is executed, e.g. the condition is resolved prior to the arithmetic logic stage calculating the target of the branch instruction. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Cocke, that Cocke's method of branching improves performance (Cocke column 1, lines 41-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the branching method of Cocke to improve processor performance.

15. Referring to claim 12, Col has taught wherein the at least one status bit is read from the memory at the same time as the digital value is read (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column

22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

16. Referring to claim 14, Col has taught wherein the at least one status bit is set high if the digital value is zero (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

17. Referring to claim 15, Col has taught wherein the at least one status bit is set high if the digital value is a positive value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

18. Referring to claim 16, Col has taught wherein the at least one status bit is set high if the digital value is negative (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52;

column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

19. Referring to claim 17, Col has taught wherein the at least one status bit is set high if the digital value is anon zero value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

20. Referring to claim 18, Col has taught wherein the at least one status bit is set high based on the value of the least significant bit of the digital value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

21. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Col et al., U.S. Patent Number 6,338,136 (herein referred to as Col) in view of Cocke et al., U.S. Patent Number 3,577,189 (herein referred to as Cocke), as applied to claims 1 and 10 above, and in further view of Olson et al., U.S. Patent Number 5,824,070 (herein referred to as Olson). Col has taught wherein the memory has one or more addressable locations (Col column 16, lines 48-53).

Col has not taught the at least one status bit is stored at the same addressable location as the corresponding digital value. Olson has taught the at least one status bit is stored at the same addressable location as the corresponding digital value (Olson column 1, lines 36-40). A person of ordinary skill in the art at the time the invention was made, and as recognized in Olson, would have recognized that the status bits must be associated with the correct instruction to be visible to the user (Olson column 1, lines 31-35). Therefore, a person of ordinary skill in the art at the time the invention was made would have incorporated the status bits of Olson in the device of Col in order to ensure the status bits are associated with the correct instruction.

Response to Arguments

22. Applicant's arguments with respect to claims 1, 3-10, and 12-18 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

23. Claims 19-27 are allowed.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

26. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
22 July 2005

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